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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

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☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 330.00

Complete if Known	
Application Number	10/078,831
Filing Date	February 18, 2002
First Named Inventor	Sanh Dang Tang
Examiner Name	M. Estrada
Art Unit	2823
Attorney Docket No.	MIO 0018 V2/40509.182/96-1138.03

METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

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2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X		=
Independent Claims		- 3** =		X		=
Multiple Dependent						=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) -0-

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY

(Complete *(if applicable)*)

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AF/2823
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicants	: Sanh Dang Tang
Serial No.	: 10/078,831
Filed	: February 18, 2002
Title	: SEMICONDUCTOR DEVICES HAVING GRADUAL SLOPE
Docket No.	: MIO 0018 V2 (96-1138.03)
Examiner	: M. Estrada
Art Unit	: 2823

Commissioner for Patents
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Susan M Luna
Agent **Reg. No. 38,769**

BRIEF ON APPEAL

This is an appeal from the Office Action mailed May 3, 2004*, finally rejecting claims 1-9 in the application. A Notice of Appeal was filed on April 30, 2004, with the accompanying fee. Our check in the amount of $330.00 accompanies this Brief in accordance with 37 CFR §1.17(c).

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventor recorded in the files of the U.S. Patent and Trademark Office at Reel 008971, Frame 0267.

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*The final rejection mailed May 3, 2004 replaced the final rejection mailed December 3, 2003. The latter rejection failed to discuss claim 9. After requesting that a new action be provided acting on all claims, applicant, upon further inquiry, was informed that the Office had misplaced this file. Applicant filed a cautionary Notice of Appeal to preserve his rights.

Related Appeals and Interferences

Applicant knows of no currently pending related appeals or interferences that would have an effect on the outcome of this appeal.

Status of Claims

Claims 1-9 are pending in this application and are before this Board for consideration on appeal. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

No amendments to the claims were filed after final rejection. All previous amendments have been entered.

Summary of the Invention

The present invention is directed to semiconductor devices having gradual slope contacts. In one embodiment of the invention, a semiconductor device precursor is provided which comprises a layer of dielectric material formed on a substrate, a layer of conductive material formed within the layer of dielectric material, and a layer of hard mask material formed on at least a portion of the dielectric material. Each of the dielectric material and layer of hard mask material have openings therein defining a via which exposes at least a portion of the layer of conductive material. An interconnect material may also be formed in the via. The layer of hard mask material includes a pair of facets, and the dielectric material includes a pair of shoulders having the hard mask material thereon.

As illustrated in Fig. 4 and described in the specification at page 7-11, the semiconductor precursor 50 includes a substrate 12 which is formed by depositing a layer 14 of dielectric insulating material 16. A layer 18 of conductive material 20 is formed on the layer 14, and a layer 22 of hard mask material 24 is formed on the layer 14. The hard mask material is then etched to expose a portion of the dielectric layer 14, form sidewalls 26 in the exposed portion of layer 14, and form a gradual slope contact. Facets 30 are then formed in the layer 22 of hard mask material by etching. The facets 30 in the layer of hard mask material together with the

sidewalls 26 of the layer 14 form a via 32A. The hard mask material which is removed during etching of the facets is redeposited along the sidewalls 26 and forms shoulders 36 on the dielectric material as illustrated in Fig. 5. Thus, all of the hard mask material formed on the dielectric layer 14 is formed from a single deposition of the same hard mask material.

As shown in Fig. 6, the layer 14 is then etched to expose a portion of the layer 18 of conductive material 20 and forms the semiconductor device precursor 50. A metal interconnect material 34 may be also be formed in the via 32 as shown in Fig. 1.

Issues Presented

The issues presented for review on appeal are:

1) Whether the Examiner erred in rejecting claims 1-6, 8 and 9 under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Blalock (U.S. 5,320,981) and Wu (5,940,731).

2) Whether the Examiner erred in rejecting claim 7 under 35 U.S.C. 103(a) as being unpatentable over Blalock and Wu and further in view of Linn et al. (5,547,596).

3) Whether the Examiner established, by evidence, a prima facie case of obviousness for any claim on appeal.

Grouping of Claims

The Examiner has made two separate grounds of rejection, rejecting claims 1-6, 8 and 9 under 35 U.S.C. 103(a) as being unpatentable over the combination of Blalock (U.S. 5,320,981) and Wu (5,940,731); and rejecting claim 7 under 35 U.S.C. 103(a) as being unpatentable over Blalock and Wu and further in view of Linn et al. (5,547,596). The application contains three rejected independent claims, namely, claims 1, 5, and 9. Applicant submits that the claims do not stand or fall together. The patentability of each independent claim will be separately argued.

The References

Blalock, U.S. Patent No. 5,320,981. Blalock teaches a method for forming a sloped contact in a layer of dielectric oxide material which utilizes a photoresist mask for etching the dielectric oxide layer. After etching, the photoresist material is removed and a second etch is performed to form a faceted edge on the dielectric layer. The dielectric material which is removed to form the facet is redeposited over a portion of the sidewall to form the desired sloping of the via.

Wu, U.S. Patent No. 5,940,731. Wu teaches a method of forming a tapered polysilicon contact plug in which a polysilicon layer is deposited on an oxide layer as a mask for etching of the oxide layer. After the oxide layer is etched, a second polysilicon layer is deposited and another etch process is performed followed by deposition of a third polysilicon layer.

Linn et al., U.S. Patent No. 5,547,896. Linn et al. teach a method of etching a thin film resistor material in which a titanium-tungsten hard mask material is deposited on an exposed surface of thin film resistor material and etched to expose the material beneath.

ARGUMENT

I. Summary of Argument

The Examiner has failed to establish a prima facie case, by evidence or reasoning, that any of the rejected claims would have been obvious with respect to the proposed combination of reference teachings. Blalock does not teach or suggest the use of a hard mask material, and there is no motivation to use a hard mask material in Blalock. Nor is there any teaching or suggestion in any of the references of a semiconductor device precursor having a layer of dielectric material including a pair of shoulders thereon which are formed from the same hard mask material which has been deposited on the dielectric material.

II. The Examiner's burden of establishing a prima facie case of obviousness has not been met.

It is well established that the burden of establishing a prima facie case of obviousness resides with the Examiner. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Piasecki*, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). This burden can be satisfied only by showing some objective teaching in the prior art, or that knowledge generally available to one of ordinary skill in the art, would lead that individual to the claimed invention. Both the teaching and a reasonable expectation of success must be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 20 USPQ2d 1438 (Fed.Cir. 1991).

Where the teachings of references are proposed to be combined, it is encumbent upon the Examiner to explain why the combination of reference teachings is proper. The suggestion to modify the reference teachings must come from the references themselves, not from applicant's disclosure. See *In re Laskowski*, 871 F.2d 115, 117, 10 USPQ2d 1397, 1398-99 (Fed. Cir. 1989); *In re Fine*, supra 837 F.2d at 1075 ("[T]eachings of references can be combined, only if there is some suggestion or incentive to do so. Here, the prior art contains none."); *Uniroyal v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 1051, 5 USPQ2d 1434 (Fed. Cir.), *cert. denied*, 109 S. Ct. 75 (1988) ("When prior art references require selective combination...to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself. Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination.") Applicant submits that the proposed combination of reference teachings here is not based on any objective teaching or suggestion in the references themselves, but rather is based on prohibited hindsight using the claimed invention as a blueprint. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985).

Applicant submits that upon close examination, the Examiner did not meet her burden of establishing a prima facie case of obviousness as to any of the claims on appeal.

III. The teachings of Blalock and Wu are not properly combinable.

In the final office action mailed May 3, 2004, the Examiner maintained the rejection of claims 1-6, 8 and 9 under 35 U.S.C. 103(a) as being unpatentable over the combination of Blalock and Wu. The Examiner has acknowledged that Blalock does not teach or suggest the use of a hard mask material formed on a dielectric layer, where the dielectric layer includes a pair of shoulders with the mask material thereon. The Examiner has also acknowledged that Blalock does not teach a layer of hard mask material having a pair of facets as claimed. However, the Examiner asserts that Wu teaches a hard mask layer (polysilicon layer 28) on a dielectric material which includes a pair of shoulders (34) and a hard mask material having a pair of facets (Fig. 6). The Examiner asserts that it would have been obvious to combine the teachings of Blalock and Wu "to enable formation of the interconnect structure."

However, the Examiner has supplied no substantive evidence or reasoning as to how or why one skilled in the art would make the proposed substitution. The desirability of the combination is clearly not suggested in the prior art. Blalock teaches a method of forming a via by redepositing **dielectric** material during etching to form sidewall spacers, while Wu teaches separate depositions of **conductive** polysilicon material to form sidewalls. The Examiner has provided no reasoning or explanation as to how or why one skilled in the art would be motivated to replace Blalock's photoresist, which is removed, with a hard mask material, which is not. Blalock redeposits a portion of the dielectric layer, not a mask layer, as recited in claim 1. Further, the Examiner has provided no reasoning or explanation as to **how** or **why** one skilled in the art would be motivated to replace Blalock's dielectric material with the electrically conductive polysilicon material taught in Wu. Claim 1, and claims 2-4 that depend therefrom, are clearly patentable because the Examiner has failed to carry her evidentiary burden.

Nor has the Examiner provided any reasoning or explanation as to why one would be motivated to combine the reference teachings for the purpose of providing an interconnect structure when Blalock does not teach or suggest a desire to form an interconnect material in his via as recited in applicant's claim 5. Claim 5, and claims 6 and 8, which depend therefrom, are patentable for this additional reason.

Further, Wu does not teach a hard mask layer which is formed by a **single deposition** of hard mask material as taught in the present invention and as recited in claim 9. The Examiner stated at page 4 of the final rejection that this limitation has not been given patentable weight, stating that "the method of forming the device is not germane to the issue of patentability of the device itself." However, applicant submits that, in this instance, the manner in which the mask material is deposited directly affects the composition of the shoulders of the claimed semiconductor device and thus must be accorded patentable weight. Wu teaches depositing **separate** layers of polysilicon material (see col. 5, line 44 to col. 6, line 25) while the present invention teaches re-deposition of the **same** mask material to form shoulders on the dielectric material. See the specification at pages 8-10. Accordingly, Wu clearly does not teach a device in which the layer of hard mask material formed on the dielectric material is the same hard mask material which forms the shoulders. This distinction is clearly set forth by applicant's recitation of a pair of shoulders having "said hard mask material thereon" in independent claims 1, 5, and 9.

Claims 1-6 and 9 are clearly patentable over the combination of Blalock and Wu.

IV. The teachings of Blalock and Wu are not properly combinable, and even if combined with Linn et al. do not render claim 7 obvious.

With regard to claim 7, which recites that the hard mask material comprises a titanium-tungsten alloy, the Examiner has cited Linn et al. for disclosing a titanium-tungsten as a hard mask material, asserting that it would have been obvious to combine Linn et al. with the teachings of Blalock and Wu "to enable formation of the hard mask layer." However, as pointed out above, Blalock does not teach a hard mask material, and there is no teaching or suggestion in Wu or Linn et al. that indicates that a tungsten-titanium alloy is interchangeable with a polysilicon mask material. Even if one were to make the proposed substitution, the claimed semiconductor device would not result as the combined teachings of the references do not teach or suggest a layer of hard mask material on a dielectric material, where the dielectric material

includes a pair of shoulders having the same hard mask material thereon. Claim 7 is clearly patentable over the cited references.

V. Conclusion

The Examiner has failed to carry her evidentiary burden of establishing a prima facie case of obviousness for any of the claims on appeal. The prior art references clearly do not render obvious the claims on appeal as they do not teach or suggest a semiconductor precursor having a layer of hard mask material which includes a pair of facets, nor do they teach or suggest a pair of shoulders on a dielectric material which are formed from the same hard mask material as claimed.

The Board is requested to reverse the rejections of claims 1-9 in their entirety.

Respectfully submitted,

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APPENDIX

The Claims on Appeal

1. A semiconductor device precursor comprising:

a substrate;

a layer of dielectric material formed on at least a portion of said substrate;

a layer of conductive material formed within said layer of dielectric material; and

a layer of hard mask material formed on at least a portion of said layer of dielectric material; at least a portion of said layer of dielectric material and said layer of hard mask material each having openings therein defining a via; said via exposing at least a portion of said layer of conductive material; said layer of dielectric material including a pair of shoulders having said hard mask material thereon; and said layer of hard mask material having a pair of facets.

2. A semiconductor device precursor as claimed in claim 1 in which said layer of hard mask material includes a layer of etch resistant material thereon.

3. A semiconductor device precursor as claimed in claim 1 wherein said hard mask material is selected from the group consisting of tungsten, tungsten silicide, poloycrystalline silicon, titanium, titanium nitride, titanium silicide, and titanium-tungsten alloys.

4. A semiconductor precursor device as claimed in claim 1, wherein said layer of conductive material contacts at least a portion of said substrate.

5. A semiconductor device precursor comprising:

a substrate;

a layer of dielectric material formed on at least a portion of said substrate;

a layer of conductive material formed within said layer of dielectric material;

a layer of hard mask material formed on at least a portion of said layer of dielectric material; at least a portion of said layer of dielectric material and said layer of hard mask material each having openings therein defining a via, said via exposing at least a portion of said layer of conductive material; said layer of dielectric material including a pair of shoulders having said hard mask material thereon, and said layer of hard mask material having a pair of facets; and

an interconnect material in said via.

6. A semiconductor device as claimed in claim 5, wherein said hard mask material is selected from the group consisting of tungsten, tungsten silicide, polycrystalline silicon, titanium, titanium nitride, titanium silicide, and titanium-tungsten alloys.

7. A semiconductor device as claimed in claim 5, wherein said hard mask material comprises a titanium-tungsten alloy.

8. A semiconductor precursor device as claimed in claim 5, wherein said layer of conductive material contacts at least a portion of said substrate.

9. A semiconductor device precursor comprising:

a substrate;

a layer of dielectric material formed on at least a portion of said substrate;

a layer of conductive material formed within said layer of dielectric material; and

a layer of hard mask material formed by a single deposition of hard mask material on at least a portion of said layer of dielectric material; at least a portion of said layer of dielectric material and said layer of hard mask material each having openings therein defining a via, said via exposing at least a portion of said layer of conductive material; said layer of dielectric material including a pair of shoulders having said hard mask material thereon, and said layer of hard mask material having a pair of facets.